APS-03-002



December 17, 2003

Commissioner for Patents P.O. Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/682,054 10/09/03

Kim Hwee Tan et al.

PILLAR STRUCTURES

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December $|^{O}$, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date ____

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"Advanced Connections," Spring 2002, Advanced Interconnect Technologies, issue describes, inter alia, a pillar bumping interconnect technology that uses perimeter or array flip-chip pads to connect an integrated circuit (IC) to a copper lead frame.

- U.S. Patent 6,550,666 to Chew et al., "Method for Forming a Flip Chip on Leadframe Semiconductor Package," discloses a method for forming a flip chip on leadframe semiconductor package.
- U.S. Patent 5,448,114 to Kondoh et al., "Semiconductor Flipchip Packaging Having a Perimeter Wall," discloses a semiconductor flip chip packaging having a perimeter wall.
- U.S. Patent 6,297,551 to Dudderar et al., "Integrated Circuit Packages with Improved EMI Characteristics," discloses integrated circuit packages with improved EMI characteristics.
- U.S. Patent 4,430,690 to Chance et al., "Low Inductance MLC Capacitor with Metal Impregnation and Solder Bar Contact," discloses a low inductance capacitor with metal impregnation and solder bar contact.

Sincerely,

Stephen B. Ackerman, Reg. No. 37761

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citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.